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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,599	02/06/2002	Ricky Merle Peterson	ROC920010319US1	8298

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EXAMINER	
SHAH, NILESH R	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,599	PETERSON, RICKY MERLE	
	Examiner	Art Unit	
	Nilesh Shah	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 states a "processor hardware thread" which is not supported in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 1, lines 8-9 it is unclear how a thread can be hardware? If the processor is accepting a thread then the thread must be software?

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chastain et al (5,050,070) (hereinafter Chastain) in view of Brenner et al (6,658,449) (hereinafter Brenner).

6. As per claim 1, Chastain teaches in the invention substantially including an apparatus comprising:

a plurality of processors, each processor having the capability of executing a plurality of threads(col. 3 lines 25-28);

a memory coupled to the plurality of processors(col. 4 lines 17-31); and

a thread dispatch mechanism residing in the memory and executed by at least one of the plurality of processors(col. 6 lines 46-52; col. 5 lines 44-50;col.17 1-39).

Chastain does not specifically teach the use of determining an idle thread.

Brenner teaches the thread dispatch mechanism determining which of the plurality of processors are idle(col. 4 lines 47-50), which of the plurality of processors can accept an

additional thread(col. 4 lines 54-56), and which of the plurality of processors cannot accept an additional thread(col. 5 lines 37-45; col. 10 lines 49-65), the thread dispatch mechanism dispatching a new thread to an idle processor, if one exists (col. 4 lines 54-56;col. 25-40).

It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Brenner and Chastain because Brenner's method of determining which processor is idle would improve Chastain's system by allowing each processor to execute threads in a high throughput manner.

7. As per claim 2, Brenner teaches an apparatus wherein, if none of the plurality of processors is idle and if at least one of the plurality of processors can accept an additional thread, the thread dispatch mechanism dispatches the new thread to one of the plurality of processors that can accept an additional thread (col. 4 lines 46-56; col. 5 lines 37-45; col. 10 lines 49-65).

8. As per claim 3, Brenner teaches an apparatus wherein, if all of the plurality of processors cannot accept an additional thread, the thread dispatch mechanism waits for one of the plurality of processors to complete processing a thread, thereby becoming a processor that can accept an additional thread, and then dispatches the thread to the processor that can accept an additional thread (col. 5 lines 37-45; col. 10 lines 49-65).

9. As per claim 4, Chastain teaches a method for dispatching threads in a computer system that includes a plurality of processors that can each execute a plurality of threads, the method comprising the steps of: determining the status of each of the plurality of processors (col. 6 lines 46-52; col. 5 lines 44-50;col.17 1-39).

   Brenner teaches wherein a processor is idle if not executing any threads, wherein the processor can accept an additional thread if busy working on one or more threads but has the capacity to process the additional thread(col. 4 lines 46-56; col. 5 lines 37-45; col. 10 lines 49-65), and wherein the processor cannot accept an additional thread if busy working on a maximum number of threads the processor can execute(col. 4 lines 47-50) and

   dispatching a new thread to an idle processor, if one exists (col. 5 lines 37-45; col. 10 lines 49-65).

10. Claims 5-6 are rejected based on the same rejection as claims 2-3 above.

11. As per claim 7, Chastain teaches a program product comprising:

    computer-readable signal bearing media bearing the thread dispatch mechanism(col. 4 lines 17-66).

    the plurality of processors cannot accept an additional thread, the thread dispatch mechanism dispatching a new thread to an idle processor(col. 6 lines 11-15; col. 10 lines 43-66; col. 5 lines 45-60).

Brenner teaches a thread dispatch mechanism that determines which of a plurality of processors in a multiprocessor computer system are idle, which of the plurality of processors can accept an additional thread(col. 4 lines 54-56), and if one exists, wherein each processor can execute a plurality of threads (col. 5 lines 37-45; col. 10 lines 49-65).

12. As per claim 8, Chastain teaches a program product wherein the computer-readable signal bearing media comprises recordable media (col. 4 lines 17-66).

13. Claim 9 is rejected based on the same rejection as claim 8 above.

14. Claims 10-11 are rejected based on the same rejection as claims 2-3 above.

15. As per claim 12 Brenner teaches an apparatus wherein all processors are made busy with a first thread before dispatching a second thread to any processor (col. 5 lines 37-45; col. 10 lines 49-65).

16. Claims 13 and 14 are rejected based on the same rejection as claim 12 above.

Response to Arguments

17. Applicant's arguments filed 9/19/05 have been fully considered but they are not persuasive. Applicant states Brenner does not teach when a processor idle to accept new threads. However, Brenner clearly teaches the a processor idle to accept new threads (col.

4 lines 44-56; col. 5 lines 37-45; col. 10 lines 49-65) ('In this way, the method assigns new threads of a new process to idle CPUs while continuing to spread the threads out across all of the nodes and CPUs.')

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hardwick (6,292,822) teaches the use of plurality of processors and threads (col.38 lines 22-44) and if an idle processor is found then assign a thread to that processor (col. 4 lines 24-67).

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh Shah whose telephone number is (571)272-3771. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah
Examiner
Art Unit 2195

NS
December 6, 2005

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